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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,740	07/25/2003	Jeong-sang Lee	Q75992	9713

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
CHERY, DADY	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,740	LEE, JEONG-SANG	
	Examiner	Art Unit	
	DADY CHERY	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 0208*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 1 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over New et al. (US Patent 4,393,457, hereinafter new) in the view of Verhenne. (US Patent 5,633,817 hereinafter Verhenne) and in further view of Wicker (US Patent 6,907,439).

Regarding claims 1, New discloses an address and data generator (Fig. 2, 42) that generates a predetermined number of write and read address (Col. 3, lines 42 –55).

New also discloses an address sequencer (26) that provides all the controls instruction to the address generator to the write addresses and the read addresses according to operation of the FFT operation (Col. 3, lines 50 – 55).

New further discloses a fast Fourier transform processor (Fig. 1) with processes signal in response to a specific instruction signal applied to the system bus (Col. 2, lines 51 – Col. 3, lines 2). New discloses the fast Fourier transform processor repeats all the butterfly operation until the transform is completed (Col.3, lines 60 –64).

But, New fails to explicitly disclose the implementing of the fast Fourier transform by using the predetermined number.

However, Verhenne teaches a Fast Fourier Transform dedicated processor that repeats data generation circuit GC to generate a predetermined number complex data sequence by using two scrambled data sequences (Abstract). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to Fast Fourier Transform (FFT) to produce a Fast Fourier Transform sequence (Abstract).

New in view of Verhenne does clearly teach if the number of addresses is generated prior to the receiving transmitted data.

However, Wicker teaches a method where the number of addresses is generated prior to the receiving transmitted data (Fig. 1A, Fig. 2, Abstract, Col. 1, lines 58 - Col. 2, lines 5 and lines 64 - Col. 3, lines 16, the number of address is determined upon a decoded value of the computation stage).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate the number of addresses prior to the receiving transmitted data for the purpose of allowing the FFT to be executed in any order desired (Col. 1, lines 59 -60).

The recitation that "A European digital audio broadcast receiver having diverse fast Fourier transform (FFT) modes based on sizes of transmitted data" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

5. Claims 2,3,6-10,12,13, 16 –20 are rejected under 35 U.S.C. 103(a) as being unpatentable over New in the view of Verhenne as applied to claim 1 above, and further in view of Mestdagh et al. (US Patent 7,010,027, hereinafter Mestdagh).

Regarding claims 2 and 12, Verhenne discloses a FFT processor that uses a predetermine number of data to produce a Fast Fourier Transform sequence (Abstract). Verhenne fails to teach the size of predetermine number of data.

However, Mestdagh teaches a FFT that use a number of 4096 data to implement a fast Fourier transform (Col. 6, lines 47 –51). This same function as described by the instant application.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider 4096 as the size of the data for system using QAM (Abstract).

Regarding claims 3 and 13, New discloses a FFT processor and an address sequencer (Memory controller) having a user- preselectable number of points that repeat and generate address data (Col. 2, lines 17 – 21). An algorithm transform unit that implemented radix-4 base operation in the case the read addresses are generated (Col. 2, lines 21 – 28). The memory controller provides a butterfly operation that is same as digit-reverse the address of the memory in the correspondence to the read addresses (Col. 3, lines 56 – 65).

New fails the specific size of the generating data. However, Mestdagh teaches a generating data of size 4096 and 2048 and implementing a Radix –4 based operations (Fig. 6 and 7, and Col. 6, lines 47 –51). This same function as described by the instant application.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider 4096 and 048 as the size of the data for system using QAM (Abstract).

Regarding claims 6 and 16, New discloses *the memory controller digit-reverses the data operated on based on the Radix-4 algorithm and stored in the memory corresponding to the FFT modes* (Col.2, lines 21 – 28).

Regarding claim 7,8,9,10,17, 18,19 and 20, New discloses the memory controller digit-reverses (butterfly operation) the bit array memory from the highest bit to the lowest bit and truncated the most significant bits to the right of the radix and appended the most significant bits to the specify address (Col. 9, lines 59 – Col. 10, lines 22). Which is substantially the same function as described by the instant application, the different FFT mode (2048, 1024, 256,512) are depend on the type of radix algorithm used.

6. Claims 4,5,14and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over New in view of Mestdagh as applied to claim 3 above, and further in view of (On computing the fast Fourier transform by Richard C. Singleton, October 1967).

Regarding claim 4, New discloses an algorithm unit that implement Radix-4 based operation (Col. 2, lines 22 – 28). Mestdagh discloses a memory that store 2048 data (Col. 6, lines 47 –51).

New in combination with Mestdagh fail to disclose the memory controller has a virtual memory. However, Richard teaches fast Fourier transform with a virtual memory system (Page 652, Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the virtual memory for the purpose of transform data sets of size exceeding the 215 words of storage (Richard page 652).

Regarding claims 5 and 15, New discloses an algorithm unit that implement Radix-4 based operation (Col. 2, lines 22 – 28).

New in combination with Mestdagh fail to disclose “0" data blocks are stored in the virtual memory in correspondence to the FFT modes. However, Richard teaches fast Fourier transform with a virtual memory system where “0” data block could be store depend on the FFT modes. (Page 652, Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the virtual memory for the purpose of transform data sets of size exceeding the 215 words of storage (Richard page 652).

Regarding claims 21 and 22, new discloses a receiver for processing data (Fig. 1 and Fig. 2), the receiver comprising:

a receiving circuit (fig.2) that receives data;

a generating circuit (42) *that generates a predetermined number of write addresses if the receiving circuit receives the data*(Col. 4, lines 50 –55); New discloses an address sequencer (36) that generates all the addresses needed for memory operation of a fast Fourier transform of a reselected length

a processing circuit (Fig. 1, 22) *that processed the received data through fast Fourier transform modes to generate a first number of data corresponding to the generated predetermined number of write addresses, wherein the processing is repeated based on a size of the received data* (Col. 1, lines 65 –66,Col. 2, lines 67 – Col.3,lines 2 and Col. 3, lines 50 –55); Where the first seed number is considered as the first number of data.

a control circuit (26) *that controls the generating circuit to generate a number of read addresses according to operations of the fast Fourier transform circuit*. New also discloses an address sequencer (26) that provides all the controls instruction to the address generator to the write addresses and the read addresses according to operation of the FFT operation (Col. 3, lines 50 – 55).

But, new fails to explicitly disclose the implementing of the fast Fourier transform by using the predetermined number.

However, Verhenne teaches a Fast Fourier Transform dedicated processor that repeats data generation circuit GC to generate a predetermined number complex data

sequence by using two scrambled data sequences (Abstract). Which is the same function as described by the instant application.

Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to Fast Fourier Transform (FFT) to produce a Fast Fourier Transform sequence (Abstract).

New in view of Verhenne does clearly teach if the number of addresses is generated prior to the receiving transmitted data.

However, Wicker teaches a method where the number of addresses is generated prior to the receiving transmitted data (Fig. 1A, Fig. 2, Abstract, Col. 1, lines 58 - Col. 2, lines 5 and lines 64 - Col. 3, lines 16, the number of address is determined upon a decoded value of the computation stage).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to generate the number of addresses prior to the receiving transmitted data for the purpose of allowing the FFT to be executed in any order desired (Col. 1, lines 59 -60).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Luo et al. (US Patent 5,491,652).

9. Rachakonda (US Patent 6976,047).

10. Deerfield et al. (US Patent 4,959,776).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DADY CHERY whose telephone number is (571)270-1207. The examiner can normally be reached on Monday - Thursday 8 am - 4 pm ESt.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2616

/Dady Chery/
Examiner, Art Unit 2616